Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently Amended) A circuit arrangement comprising:

a complementary pass transistor logic;

a static driver ~~connected~~ coupled to the complementary pass transistor logic and ~~driving~~ configured to drive complementary input nodes to each other of the complementary pass transistor logic by a low swing voltage, the static driver including a PMOS transistor and an NMOS transistor ~~provided~~ which are coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal; and

a charge recycling circuit ~~connected~~ coupled to the complementary pass transistor logic and ~~performing~~ configured to perform charge sharing between the complementary input nodes when the complementary pass transistor logic is not driven by the static driver.

Claim 2. (Original) The circuit arrangement as claimed in claim 1, wherein a swing level of the low swing voltage ranges from a ground voltage level to a supply voltage level minus a threshold voltage level.

Claim 3. (Currently Amended) The circuit arrangement as claimed in claim 1, wherein the static driver is formed of a plurality of transistors ~~connected~~ coupled in series.

Claim 4. (Currently Amended) A low swing charge recycling circuit arrangement comprising:

a complementary pass gate stage having driving inputs to receive each of driving input signals, having complementary outputs to produce an output signal on one hand and a complementary output signal on the other and determining a logic operation of the circuit arrangement;

a static low swing driver stage having a signal input to receive an input signal, having a clock input to receive a clock signal, and having complementary outputs to produce low swing complementary signals to each output to be provided to the driving inputs of the complementary pass gate stage when the clock signal is in one of two states, the static driver stage including a PMOS transistor and an NMOS transistor ~~provided~~ which are coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal; and

an equalization stage ~~being connected~~ coupled to the complementary outputs, having a clock input to receive the clock signal and producing complementary signals to the driving inputs of the complementary pass gate stage when the clock signal is in the other state, whereby a charge shared a signal of an intermediate voltage level between those of the complementary outputs is shared between the driving inputs.

Claim 5. (Currently Amended) An adder comprising:

a carry propagating circuit ~~for~~ configured to alternatively ~~propagating~~ propagate low swing driven complementary carry input signals and charge sharing complementary carry input signals;

a static low swing driver circuit ~~receiving~~ configured to receive generate signals and ~~producing~~ to produce low swing driven complementary generate signals, the static driver circuit including a PMOS transistor and an NMOS transistor ~~provided~~ which are coupled between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal;

a pass gate network ~~receiving~~ configured to receive the complementary carry input signals, the complementary generate signals and propagate signals and being controlled by the propagate signals ~~for producing~~ to produce a sum signal by applying XOR operation to the complementary carry input signals with the propagate signals;

an equalization circuit ~~adapted~~ configured to be operative alternatively with the static low swing driver circuit and ~~providing~~ to provide charge sharing complementary generate signals to the pass gate network; and

a latch circuit ~~connected~~ coupled to the pass gate network and ~~latching~~ configured to latch the produced sum signal.

Claim 6. (Currently Amended) An adder module comprising:

at least one adder ~~connected~~ coupled in series, each adder being provided on the basis of one bit to be added; and

a carry input signal equalization circuit ~~receiving~~ configured to receive carry input signals and ~~providing~~ to

provide charge sharing complementary carry input signals to one end of the adders ~~connected~~ coupled in series,

wherein the adder ~~includes~~ comprises:

a carry propagating circuit ~~for~~ configured to alternatively ~~propagating~~ propagate low swing driven complementary carry input signals and the charge sharing complementary carry input signals;

a static low swing driver circuit ~~receiving~~ configured to receive generate signals and ~~producing~~ to produce low swing driven complementary generate signals, the static driver circuit including a PMOS transistor and an NMOS transistor ~~provided~~ which are coupled between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal;

a pass gate network ~~receiving~~ configured to receive the complementary carry input signals, the complementary generate signals and propagate signals and being controlled by the propagate signals ~~for producing~~ to produce a sum signal by applying XOR operation to the complementary carry signals with the propagate signals ~~with the propagate signals~~;

an equalization circuit ~~adapted~~ configured to be operative alternatively with the static low swing driver circuit and ~~providing~~ to provide charge sharing complementary generate signals to the pass gate network; and

a latch circuit ~~connected~~ coupled to the pass gate network and ~~latching~~ configured to latch the produced sum signal.

Claim 7. (Currently Amended) The adder module as claimed in claim 6 further comprising:

a carry propagating path ~~for propagating~~ configured to propagate the complementary carry input signals in series of bits;

a carry skip path ~~bypassing~~ configured to bypass the adders ~~connected~~ coupled in series in order to pass the complementary carry input signals transparently; and

a carry conflict-free circuit ~~for protecting~~ configured to protect a conflict of the propagated carry input signals and the passed carry input signals.

Claim 8. (New) A circuit arrangement comprising:

a complementary pass transistor logic;

a static driver coupled to the complementary pass transistor logic and configured to drive complementary input nodes to each other of the complementary pass transistor logic by a low swing voltage, wherein the static driver comprises a PMOS transistor and an NMOS transistor, a voltage swing level of the static driver changes in at least one of (i) from ground level to $V_{dd} - V_{th}$ and (ii) from V_{th} to V_{dd}, V_{dd} denoting a supply voltage and V_{th} denoting a threshold voltage of the NMOS transistor; and

a charge recycling circuit coupled to the complementary pass transistor logic and configured to perform charge sharing between the complementary input nodes when the complementary pass transistor logic is not driven by the static driver.